CLAIMS

What is claimed is:

1. A programmable buffer circuit for interfacing a CPU to a plurality of channel interfaces, comprising:

a dual port memory having a first port coupled to a CPU data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;

an arbitrator for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus;

an address generator for generating dual port memory addresses for reading and writing data using said CPU data bus and said channel data bus; and

an allocator and control unit programmable by said CPU for specifying individual ones of buffer locations and sizes within said dual port memory for individual ones of said channel interfaces, and for enabling individual ones of said buffers, said allocator having outputs coupled to said address generator for controlling the generation of addresses thereby depending on which channel interface is currently selected for access to said dual port memory.

2. A programmable buffer circuit as in claim 1, wherein said control unit is programmable for operating individual ones of channel buffers in a block access mode or in a first in/first out (FIFO) access mode of operation.

3. A programmable buffer circuit as in claim 1, wherein at least said dual port memory, said CPU and said plurality of interface channels are contained within a common integrated circuit package.

4. A programmable buffer circuit as in claim 1, wherein one of said plurality of interface channels is comprised of an audio CODEC.

5. A programmable buffer circuit as in claim 1, wherein one of said plurality of interface channels is comprised of a serial data interface.

6. A programmable buffer circuit as in claim 1, wherein one of said plurality of interface channels is comprised of a packet data interface channel.

7. A programmable buffer circuit as in claim 1, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein said allocator comprises a corresponding plurality of registers for specifying at least a starting address and a size for each of of said receive interface and said transmit interface.

8. A programmable buffer circuit as in claim 1, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein said buffer circuit is programmable for specifying a receive buffer of one channel interface to be a transmit buffer of another channel interface.

9. A method for operating a programmable buffer circuit for interfacing a CPU to a plurality of channel interfaces, comprising step of:

providing a dual port memory having a first port coupled to a CPU data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;

programming a control unit for specifying individual ones of buffer locations and sizes within said dual port memory for individual ones of said channel interfaces;

arbitrating for access to said dual port memory by individual ones of said channel interfaces over said channel data bus; and

generating dual port memory addresses for reading and writing data using said CPU data bus and said channel data bus, the generation of said addresses depending on which channel interface is currently selected for access to said dual port memory, and on the specified buffer location and size within said dual port memory for the selected one of said channel interfaces.

10. A method as in claim 9, wherein said step of programming further specifies for individual ones of channel buffers whether the channel buffer is operated in a block access mode or in a first in/first out (FIFO) access mode of operation.

11. A method as in claim 9, wherein at least said dual port memory, said CPU and said plurality of interface channels are contained within a common integrated circuit package.

12. A method as in claim 9, wherein one of said plurality of interface channels is comprised of an audio CODEC, and wherein another one of said plurality of interface channels is comprised of at least one of a serial data interface and a packet data interface.

13. A method as in claim 9, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein said step of programming specifies at least a starting address and a size for each of said receive interface and said transmit interface.

14. A method as in claim 9, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein said step of programming specifies a receive buffer of one channel interface to be a transmit buffer of another channel interface.

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